In the United States Patent and Trademark Office

In re the application of
Hashimoto, et al. TI-12592A.23

Serial No. 10/816,076 Art Unit: 2188

Filed: 3/31/2004 Examiner: J. Lane

Title: Synchronous DRAM System with Control Data

Information Disclosure Statement A, B, C, and D

December 7, 2004

Asst. Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Asst. Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 7, 2004.

Lawrence J. Bassuk, Reg. No. 29,043

Dear Sir:

Applicants request consideration of the patents and other documents listed on enclosed forms PTO-1449.

Applicants combine four Information Disclosure Statements to bring art to the attention of the examiner. In previous applications, these four Information Disclosure Statements had been submitted separately. The separate statements identified the source of the listed references, as follows:

Information Disclosure Statement A had listed art from ancestor applications to this application, listed art from a later filed application for a synchronous DRAM and listed other patents owned by the assignee Texas Instruments Incorporated;

Information Disclosure Statement B had listed art cited in a search requested by Texas Instruments and conducted by the European Patent Office;

Information Disclosure Statement C had listed art cited in U. S. Patent 5,319,755 to Farmwald and assigned to RAMBUS, Inc.; and

Information Disclosure Statement D had listed art cited in U. S. Patent 4,789,960 to Willis, cited in the European search.

Each of the attached Forms 1449 identifies one of the above described Information Disclosure Statements as the source of the listed art.

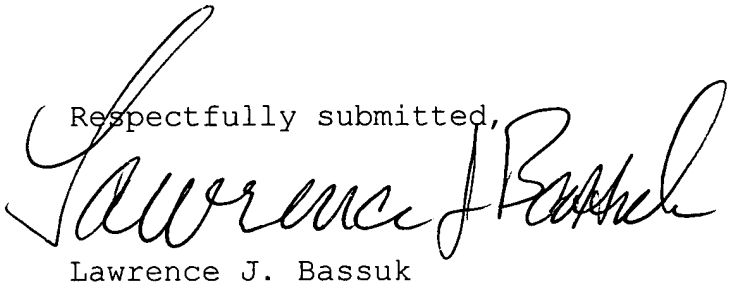
Under 37 CFR 1.98(d), no copy of the cited art is provided in this application. A copy of the cited art was previously cited and submitted to the Office in application Number 08/362,289, filed December 22, 1994. That application is relied upon for an earlier filing date under 35 U.S.C. 120.

Concise explanations of the listed patents and other documents that disclose a clock signal applied to or received by a memory part occur in Attachment A. Applicants' undersigned representative has looked at every listed reference and applicants believe that they have noted every patent or other document that discloses a clock signal applied to or received by a memory part; applicants cannot exclude however the possibility of unintentionally missing some such disclosure.

Under Rule 97(h), the filing of this information disclosure statement shall not be construed to be an admission that the information cited in this statement is, or is considered to be material to patentability as defined in Rule 56(b).

Please consider this statement as being filed under Rule 97(c), after the period specified in Rule 97(b), but before the mailing date of either a final action, or a notice of allowance. Under Rule 97(c), applicant submits the fee set forth in Rule 17(p). Please charge the fee under Rule 17(p) of $130.00 to Deposit Account Number 20-0668 of Texas Instruments Incorporated. We enclose two copies of this sheet.

Respectfully submitted,



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INFORMATION DISCLOSURE STATEMENT A

FORM PTO-1449 (REV. 7-80)

U.S. DEPARTMENT OF COMMERCE
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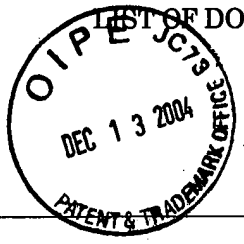
LIST OF DOCUMENTS CITED BY APPLICANT

(Use several sheets if necessary)



ATTY. DOCKET NO.	SERIAL NO.
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FILING DATE: March 31, 2004	GROUP: 2188

U.S. PATENT DOCUMENTS

+EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		3,895,360	07/15/75	Cricchi, et al.	340	173R	01/29/74
		3,962,689	06/08/76	Brunson	340	173R	11/21/74
		4,120,048	10/10/78	Fuhrman	365	239	12/27/77
		4,321,695	03/23/82	Redwine, et al.	365	174	11/23/79
		4,509,142	04/02/85	Childers	364	900	12/15/82
		4,581,721	04/08/86	Gunawardana	365	230	10/25/82
		4,608,678	08/26/86	Threewitt	365	189	09/28/84
		4,633,441	12/30/86	Ishimoto	365	189	09/28/84
		4,796,224	01/03/89	Kawai et al	365	51	02/17/87
		4,833,651	05/23/89	Seltzer, et al.	365	189.07	05/23/98
		4,999,814	03/12/91	Hashimoto	365	222	08/07/87
		4,567,579	01/28/86	Patel et al.	365	189	07/08/83
		4,618,947	10/21/86	Tran et al.	365	230	07/26/84
		4,685,089	08/04/87	Patel et al.	365	233	08/29/84

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FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
		59 56276	9/24/1982	Japan	G 11 C	8/00	X

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LIST OF DOCUMENTS CITED BY APPLICANT *(Use several sheets if necessary)*		TI-12592A.23	10/816,076
		APPLICANT Hashimoto, et al.	
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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*			
		Bell Laboratories, Incorporated, Transmission Systems for Communications, 5th Edition, 1982, pp. 590-591.	
		Cole, Bernard C., "Motorola's Radical SRAM Design Speeds Systems 40%, Electronics", July 23, 1987, pp. 66-68.	
		Hashimoto, Masashi et al., "A 20-ns 256K X 4 FIFO Memory", IEEE Journal of Solid-State Circuits, Vol. 23, No. 2, April 1988, pp. 490-499.	
		Hashimoto, Masashi et al., "A 20 ns 256K X 4 FIFO Memory", IEEE 1987 Custom Integrated Circuits Conference, May 4-7, 1987, pp. 315-318.	
		Horowitz, Mark et al., "MIPS-X: A 20-MIPS Peak, 32-bit Microprocessor with On-Chip Cache", IEEE Journal of Solid-Circuits, Vol. SC-22, No. 5, October 1987, pp. 790-799.	
		Lineback, J. Robert, "System Snags Shouldn't Slow the Boom in Fast Static RAMS", Electronics, July 23, 1987, pp. 60-62.	
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		Motorola, "16Kx4 Bit Synchronous Statis RAM with Output Registers and Output Enable", Motorola Semiconductor Technical Data, MCM6294.	
		Nakagawa et al., "A 1 Mb Field Memory For TV Pictures", IEEE 1987 Custom Integrated circuits Conference, Pages 319-322.	
		Ohara, Kazuhiro et al., "A Field Store System With Single 1Mbit Field Memory, ICCE Digest of Technical Papers", pages 70-71, June, 1988.	
		Wada, R. et al., "A Color Television Receiver With Digital Frame Memory", 1966 IEEE Transactions on Consumer Electronics, Vol. 4, No. 3, pages 128-129.	

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+EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		4,549,283	10/22/85	McDermott, III	365	194	09/06/83
		4,899,316	02/06/90	Nagami	365	189.01	12/29/86

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		0,147,268 A2	07/1985	Europe	G 11 C	8/00	X
		0,276,870 A2	07/1985	Europe	G 11 C	8/00	X
		62 152 050	07/1987	Japan	G 06 F	12/00	X
		0,162,234 A2	11/1985	Europe	G 11 C	8/00	

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INFORMATION DISCLOSURE STATEMENT C

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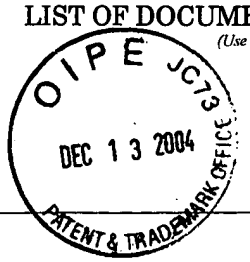

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+EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
		3,740,723	06/1973	Beausoleil et al	395	425	
		3,758,761	09/1973	Henrion	371	8.1	
		3,771,145	11/1973	Wiener	365	240	
		3,821,715	06/1974	Hoff et al.	340	173	
		3,882,470	05/1975	Hunter	364	200	
		3,924,241	12/1975	Kronies	395	425	
		3,969,706	07/1976	Proebsting et al.	365	189.02	
		3,972,028	07/1976	Weber et al.	395	425	
		3,975,714	08/1976	Weber et al.	395	800	
		3,983,537	09/1976	Parsons et al.	395	425	
		4,007,452	02/1977	Hoff	365	63	
		4,038,648	07/1977	Chesley	365	201	
		4,099,231	07/1978	Kotok et al.	395	425	
		4,191,996	03/1980	Chesley	395	425	
		4,205,373	05/1980	Shah	395	425	
		4,247,817	01/1981	Heller	307	354	
		4,249,247	02/1981	Patel	395	425	
		4,286,321	08/1981	Baker et al.	364	200	
		4,306,298	12/1981	McElroy	395	425	
		4,315,308	02/1982	Jackson	364	200	
		4,333,142	06/1982	Chesley	395	500	
		4,355,376	10/1982	Gould	365	200	
		4,373,183	02/1983	Means et al.	395	400	
		4,385,350	05/1983	Hansen et al.	365	229	
		4,443,864	04/1984	McElroy	395	325	
		4,449,207	05/1984	Kung et al.	365	189.02	
		4,468,738	08/1984	Hansen et al.	395	325	
		4,470,114	09/1984	Gerhold	395	325	
		4,481,625	11/1984	Roberts et al.	370	85	
		4,488,218	12/1984	Grimes	395	325	
		4,500,905	02/1985	Shibata	357	68	
		4,519,034	05/1985	Smith et al.	395	550	
		4,595,923	06/1986	McFarland, Jr.	340	825.5	

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		4,630,193	12/1986	Kris	395	325	
		4,646,270	02/1987	Voss	365	189.02	
		4,649,511	03/1987	Gdula	395	425	
		4,649,516	03/1987	Chung et al.	395	250	
		4,654,655	03/1987	Kowalski	340	825.5	
		4,706,166	11/1987	Go	361	403	
		4,719,627	01/1988	Peterson et al.	371	40.2	
		4,745,548	05/1988	Blahut	395	425	
		4,764,846	08/1988	Go	361	388	
		4,770,640	09/1988	Walter	439	69	
		4,779,089	10/1988	Theus	340	825.5	
		4,785,394	11/1988	Fischer	395	325	9/1986
		4,811,202	03/1989	Schabowski	395	325	10/1981
		4,818,985	04/1989	Ikeda	340	825.5	11/1987
		4,837,682	06/1989	Culler	395	325	4/1987
		4,860,198	08/1989	Takenaka	364	200	9/1985
		4,933,835	06/1990	Sachs et al.	364	200	1/1989
		4,975,763	12/1990	Baudouin et al.	357	74	3/1988
		5,023,488	06/1991	Gunning	307	475	3/1990
		5,179,670	01/1993	Farmwald et al.	395	325	12/1989
		5,319,755	06/1994	Farmwald et al.	395	325	4/1990

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

		Hawley, David, "Superfast Bus Supports Sophisticated Transactions," High Performance Systems, Sep. 1989.	
		T. Yang, M. Horowitz, B. Wooley, "A 4-ns 4KX1-bit Two-Port BiCMOS SRAM," IEEE Journal of Solid-State Circuits, Vol. 23, No. 5, pp. 1030-1040 (Oct. 1988).	
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		Agarwal et al., "An Analytical Cache Model," ACM Trans. on Computer Systems, Vol. 7 No.2, pp. 184-215 (May 1989).	
		Davidson, "Electrical Design of a High Speed Computer Package", IBM J. Res. Develop., Vol. 26, No. 3, pp. 349-361 (1982).	
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		Horowitz et al., "MIPS-X: A 20-MIPS Peak 32-Bit Microprocessor with ON-Chip Cache," IEEE J. Solid State Circuits, Vol. SC-22, No. 5, pp. 790-799 (Oct. 1987).	
		Kwon et al., "Memory Chip Organizations for Improved Reliability in Virtual Memories," IBM Technical Disclosure Bulletin, Vol. 25, No. 6, November 1982, pp. 2952-2957.	
		Pease et al., "Physical Limits to the Useful Packaging Density of Electronic Systems," IBM J. Res. Develop. Vol. 32 No. 5, (Sep, 1988).	
		Peterson, "System-Level Concerns Set Performance Gains," High-Performance Systems, pp. 71-77 (Sep. 1989).	

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		Wooley et al., "Active Substrate System Integration," Private Communication, Semiconductor Research Corporation, 4 pages (Mar. 15, 1988).	
		H. Schumacher, "CMOS Subnanosecond True-ECL Output Buffer," IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, pp. 150-154 (Feb. 1990).	

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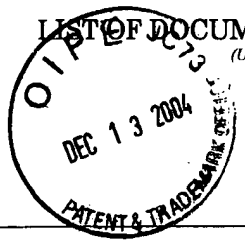

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		3,956,737	05/11/76	Ball	340	172.5	07/12/74
		4,152 ,781	05/01/79	Aichelmann, Jr.	365	239	06/30/78
		4,225,947	09/30/80	Councill et al.	365	238	12/29/78
		4,375,084	03/22/83	Urushibata	364	900	06/29/79
		4,388,696	06/14/83	Test, II et al.	364	900	07/14/80
		4,415,994	11/15/83	Ive et al.	365	189	09/14/81
		4,435,792	03/06/84	Bechtolsheim	365	230	06/30/82
		4,493,060	01/08/85	Varshney	365	238	10/29/83
		4,558,377	12/10/85	Collins et al.	360	10.1	05/05/82
		4,608,669	08/26/86	Klara et al.	365	201	05/18/84
		4,664,502	02/17/87	Kawashima	365	219	03/26/84
		4,667,313	05/19/87	Pinkham et al.	365	240	0122/85
		4,789,960	12/06/88	Willis	364	900	01/30/87

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INFORMATION DISCLOSURE STATEMENT D

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		Kimura et al., "Power Reduction Techniques in Megabit DRAM's", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 3, June 1968.	
		Nogami et al., "1-Mbit Virtually Static RAM, IEEE Journal of Solid-State Circuits", Vol. SC-21, No. 5, October 1986.	
		Ohta et al., "A 1-Mbit DRAM with 33-MHz Serial I/O Ports", IEEE Journal of Solid-State Circuits, Vol. SC-21, No. 5, October 1986.	

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